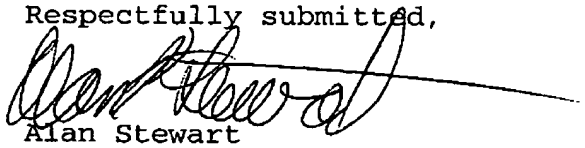
REMARKS

Claims 1-28 are pending in the application. Claims 1-28 are rejected.

Claims 1-28 were rejected under 35 USC 102(b) as anticipated by Kimura. Claims 1-28 include a lower-order accumulator chain for processing only lower order bits and a higher-order accumulator chain for processing only higher-order bits. The references of record do not show, teach, or suggest these limitations. The Kimura reference does not show, teach, or suggest the accumulator chains of Claims 1-28. The Kimura reference discloses an addition circuit for adding feedback digital data to input data. The Kimura reference does not show accumulator chains. Therefore, claims 1-28 are believed to be allowable over the references of record.

It is believed that the above remarks are fully responsive to the Official Action. Reconsideration and allowance are therefore respectfully requested.

Respectfully submitted,



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